

**REMARKS**

Claims 1-9 are pending. The Final Action dated December 29, 2003 has been carefully considered. The above amendments and the following remarks are presented in a sincere attempt to place this application in condition for allowance. Claims 1 and 2 have been amended in this Response. The Examiner states that Claims 3-9 are allowable over the prior art of record, for which Applicant thanks the Examiner. (Office Action, page 5.) Reconsideration and allowance are respectfully requested in light of the foregoing amendments and the following remarks.

Claim 1 stands rejected under 35 U.S.C. §102(b) in view of U.S. Patent No. 5,418,486 by Callahan ("Callahan"). Insofar as it may be applied against the Claim, this rejection is overcome. Specifically, Callahan was cited as assertedly fully disclosing the following: (1) applying one of the pair of pulse width modulated signals both to a set input of a latch circuit and to a delay circuit; (2) applying the other of the pair of pulse width modulated signals to a reset input of the latch circuit, wherein both of the pair of pulse width modulated signals have substantially constant and equidistant start transition times; and (3) obtaining a constant width drive signal from the output of said latch circuit.

Rejected independent Claim 1 as now amended more particularly recites one of the distinguishing characteristics of the present invention, namely, "obtaining a second pulse width modulated drive signal from an output of the delay circuit." Support for this Amendment can be found, among other places, page 6, line 17 to page 8, line 5 and FIGURES 1 and 2 of the original Application.

Callahan does not suggest, teach, or disclose a pulse width modulated signal output in conjunction with a constant pulse width signal output. Specifically the Examiner states on page 2 of the Office Action that the outputs of the circuit of FIGURE 2 of Callahan are Q and Qbar of an RS

Flip-Flop. The above-referenced Application also states, on page 6, lines 22-26, "the circuits 10 and 14, of FIGURE 1, operate in the manner of set/reset latch circuits or of toggle circuits which are caused to change output levels with each positive transition of either one of input signals A and B to produce constant width (non-PWM) output drive signals." Each output of each of the circuits 10 and 14 has both an output and an inverted output similar to the outputs of the latch of Callahan. However, the above-referenced Application also details an outputted pulse width modulated, provided by delay circuits, such as 12 and 16, in conjunction with the constant width signal in FIGURES 1 and 2. Therefore, Callahan does not teach, suggest or disclose outputting a pulse width modulated signal in conjunction with constant width signals that is capable of driving certain devices, such as DC-to-DC converters. By utilizing the multiple outputs that can effectively drive certain devices, such as DC-to-DC converters, as the present invention of Claim 1 recites, better control can be achieved of power conversion for such devices as DC-to-DC converters utilizing full wave bridges, for example.

In view of the foregoing, it is apparent that the cited reference does not disclose, teach or suggest the unique combination now recited in amended Claim 1. Applicant therefore submits that amended Claim 1 is clearly and precisely distinguishable over the cited reference in a patentable sense, and is therefore allowable over this reference and the remaining references of record. Accordingly, Applicant respectfully requests that the rejection of amended Claim 1 under 35 U.S.C. § 102(b) in view of Callahan be withdrawn and that Claim 1 be allowed.

Claim 2 stands rejected under 35 U.S.C. §102(b) in view of Callahan. Insofar as it may be applied against the Claim, this rejection is overcome. Specifically, Callahan was cited as assertedly fully disclosing the following: (1) a first pulse width modulated control signal supplying means connected at least to a delay circuit; (2) a second pulse width modulated control signal supplying

means, wherein both of the pair of pulse width modulated control signal supplying means have substantially constant and equidistant start transition times; (3) a toggle circuit, connected to said first and second control signal supplying means, the toggle circuit supplying a first output drive signal level upon detecting a given characteristic of a first pulse width modulated control signal received from said first supplying means and supplying a second output drive signal level upon detecting said given characteristic of a second pulse width modulated control signal received from said second supplying means, whereby substantially symmetrical first and second output drive signals are generated from said toggle circuit.

Applicant contends that the rejection of amended Claim 2 is overcome for at least some of the reasons that the rejection of Claim 1 as amended is overcome. These reasons include Callahan not disclosing, teaching, or suggesting "a delay circuit connected at least to the first pulse width modulated control signal supplying means, wherein the delay circuit at least provides a pulse width modulated drive signal." Applicant therefore respectfully submits that amended Claim 2 is clearly and precisely distinguishable over the cited references in any combination.

In view of the foregoing, it is apparent that the cited reference does not disclose, teach or suggest the unique combination now recited in amended Claim 2. Applicant therefore submits that amended Claim 2 is clearly and precisely distinguishable over the cited reference in a patentable sense, and is therefore allowable over this reference and the remaining references of record. Accordingly, Applicant respectfully requests that the rejection of amended Claim 2 under 35 U.S.C. § 102(b) in view of Callahan be withdrawn and that Claim 2 be allowed.

Applicants have now made an earnest attempt to place this application in condition for allowance. For the foregoing reasons and for other reasons clearly apparent, Applicants respectfully request full allowance of Claims 1 through 9.

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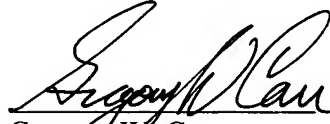
PATENT APPLICATION  
SERIAL NO. 10/077,408

Applicant does not believe that any fees are due; however, in the event that any fees are due, the Commissioner is hereby authorized to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 50-0605 of Carr LLP.

Should the Examiner deem that any further amendment is desirable to place this application in condition for allowance, the Examiner is invited to telephone the undersigned at the number listed below.

Respectfully submitted,

CARR LLP

  
Gregory W. Carr  
Reg. No. 31,093

Dated: 3/31/04  
CARR LLP  
670 Founder's Square  
900 Jackson Street  
Dallas, Texas 75202  
Telephone: (214) 760-3030  
Fax: (214) 760-3003